



Pipelined Architecture

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Contents

- Basic definitions
- Different signals used
- Bus cycle definition
- Address pipelining
- Read write cycles
- Non-pipelined machine cycle
- Pipelined machine cycle

Basic Definitions

- Clock: Processor clock (one processor clock period = two CLK2 periods)
- Bus state: The shortest time unit of bus activity (T1: Address & Status active, T2: Data transfer)
- Bus cycle: is the basic mechanism for information transfer, either from system to processor, or from processor to system.
- The Bus: Collection of the address bus, data bus and all associated control signals

Different Signals used

- **Note:** # symbol at the end of a signal name indicates the active, or asserted, state occurs when the signal is at a low voltage
- **CLK2:** provides fundamental timing, divided by two to generate internal processor clock used for instruction execution. The internal clock comprises two phase: phase 1 & phase 2
- **Address Bus (BE0# through BE3#, A2 through A31):** These three-state outputs provide physical memory addresses or I/O port addresses. BE0# - BE3#, directly indicate which bytes of the 32-bit data bus are involved with the current transfer

Different Signals used

Continued...

- **DATA BUS (D0 through D31):** These three-state bidirectional signals provide the general purpose data path
- **ADDRESS STATUS (ADS#):** This three-state output indicates that a valid bus cycle definition, and address (W/R#, D/C#, M/IO#, BE0# - BE3#, and A2 - A31) is being driven at the Intel386 DX pins. It is asserted during T1 and T2P bus states.
- **NEXT ADDRESS REQUEST (NA#):** This is used to request address pipelining.
- **TRANSFER ACKNOWLEDGE (READY#):** This input indicates the current bus cycle is complete, and the active bytes indicated by BE0# - BE3# and BS16# are accepted or provided

Different Signals used

Continued...

- **BUS SIZE 16 (BS16#):** The BS16# feature allows the Intel386 DX to directly connect to 32-bit and 16-bit data buses. Uses only the lower-order half (D0 - D15) of the data bus, corresponding to BE0# and BE1#.
- **W/R#:** distinguishes between write and read cycles.
- **D/C#:** distinguishes between data and control cycles.
- **M/IO#:** distinguishes between memory and I/O cycles.
- **LOCK#:** distinguishes between locked and unlocked bus cycles.

Bus Cycle Definition

- Bus Cycle Definition Signals (W/R#, D/C#, M/IO#, LOCK#)

M/IO #	D/C #	W/R #	Bus Cycle Type
Low	Low	Low	INTERRUPT ACKNOWLEDGE
Low	Low	High	does not occur
Low	High	Low	I/O DATA READ
Low	High	High	I/O DATA WRITE
High	Low	Low	MEMORY CODE READ
High	Low	High	<div> <div> HALT: Address = 2 </div> <div> SHUTDOWN: Address = 0 </div> </div> <hr/> <div> <div> (BE0# High BE1# High BE2# Low BE3# High A2-A31 Low) </div> <div> (BE0# Low BE1# High BE2# High BE3# High A2-A31 Low) </div> </div>
High	High	Low	MEMORY DATA READ
High	High	High	MEMORY DATA WRITE

Address Pipelining

- Provides a choice of bus cycle timings.
- Pipelined or non-pipelined address timing is selectable on a cycle-by-cycle basis with the Next Address (NA#) input.
- When address pipelining is not selected, the current address and bus cycle definition remain stable throughout the bus cycle.
- When address pipelining is selected, the address (BE0# - BE3#, A2 - A31) and definition (W/R#, D/C# and M/IO#) of the next cycle are available before the end of the current cycle.

Address Pipelining

Continued...

- The fastest bus cycles using pipelined address require only two bus states, named T1P and T2P.
- Therefore cycles with pipelined address timing allow the same data bandwidth as non-pipelined cycles, but address-to-data access time is increased compared to that of a non-pipelined cycle.
- By increasing the address-to-data access time, pipelined address timing reduces wait state requirements.

Read and Write Cycles

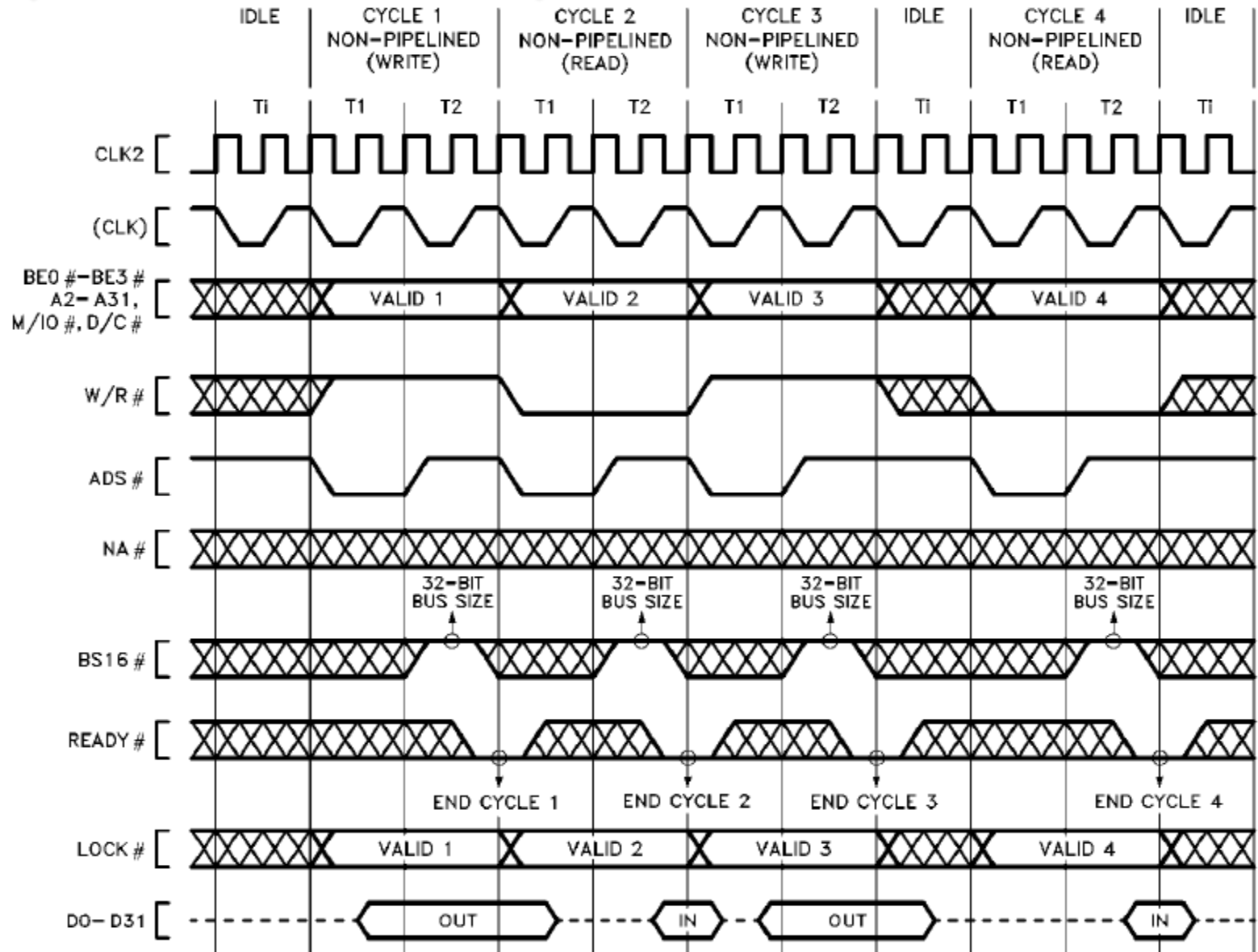
- Data transfers occur as a result of bus cycles, classified as read or write cycles.
- Two choices of address timing are dynamically selectable: non-pipelined, or pipelined.
- After a bus idle state, the processor always uses non-pipelined address timing.
- However, the NA# (Next Address) input may be asserted to select pipelined address timing for the next bus cycle.
- When pipelining is selected and the Intel386 DX has a bus request pending internally, the address and definition of the next cycle is made available even before the current bus cycle is acknowledged by READY#.

Read and Write Cycles

Continued...

- Terminating a read cycle or write cycle, like any bus cycle, requires acknowledging the cycle by asserting the READY# input.
- Until acknowledged, the processor inserts wait states

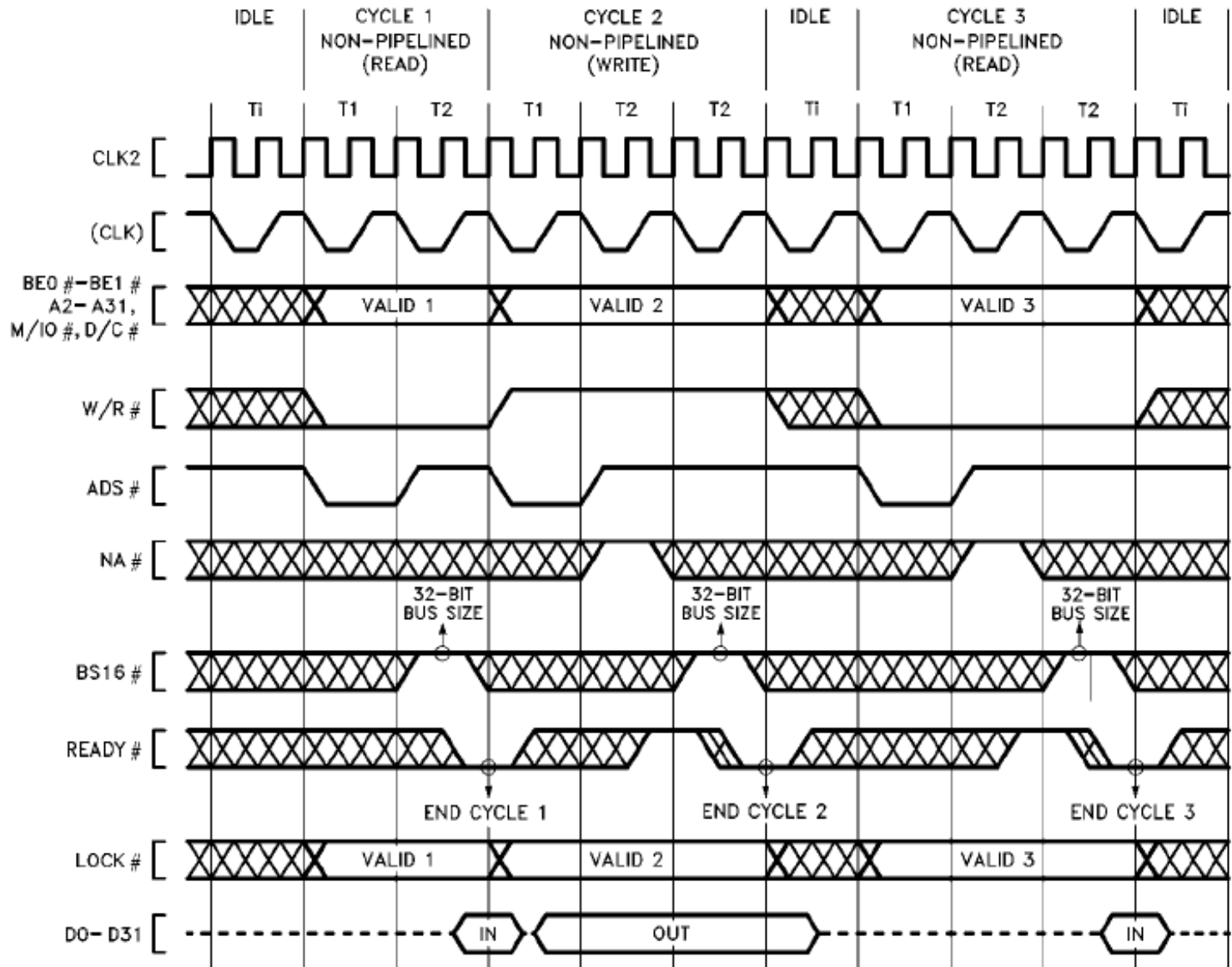
Non-pipelined read & write cycles (No wait states)



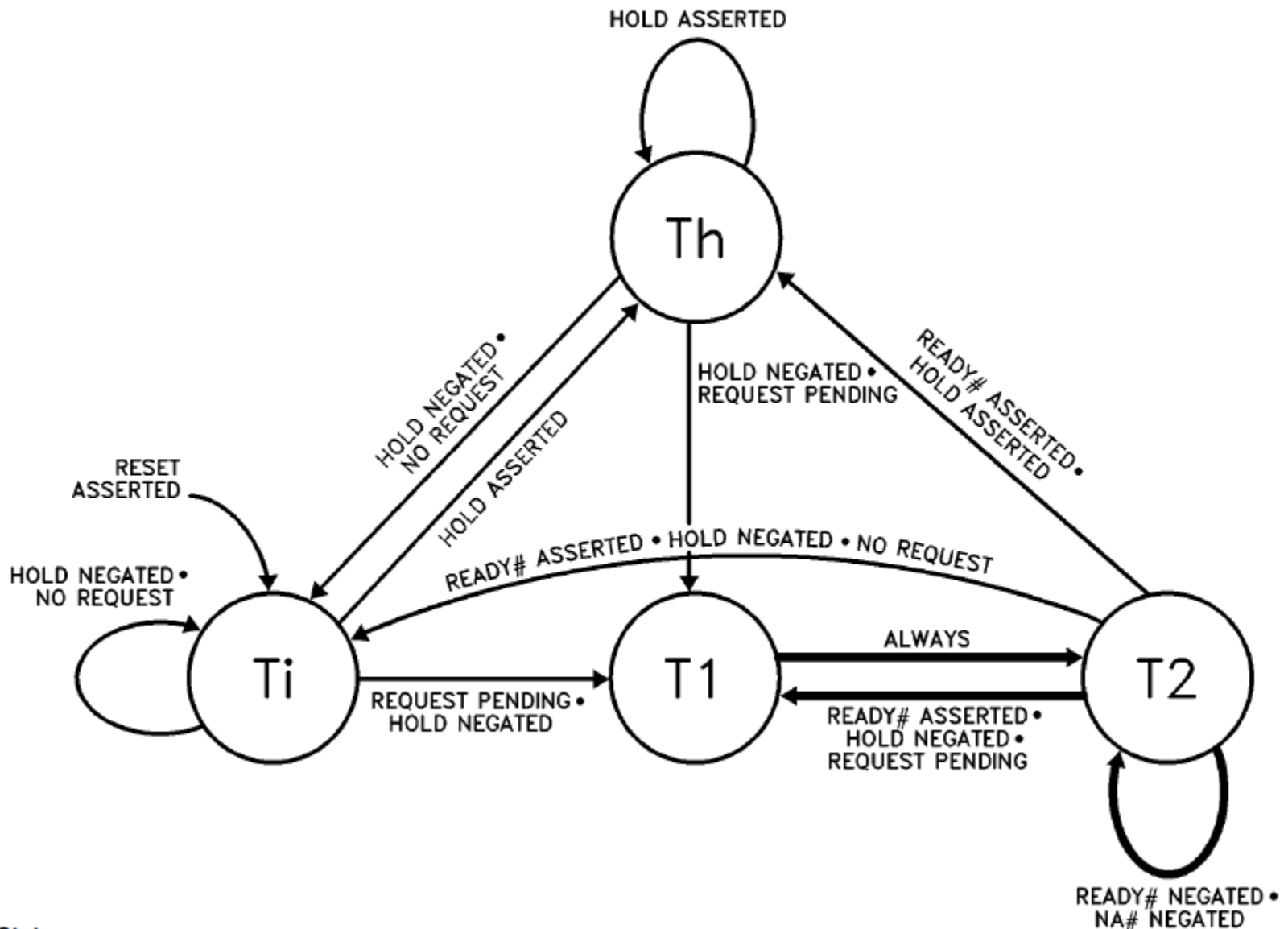
Non-pipelined read & write cycles

- At the end of the second bus state within the bus cycle, READY# is sampled
- If asserted the bus cycle terminates
- Else the cycle continues another bus state (a wait state) and READY# is sampled again at the end of that state.
- This continues indefinitely until the cycle is acknowledged by READY# asserted.

Non-pipelined read & write cycles (With wait states)



Bus States (Using non-pipelined address)

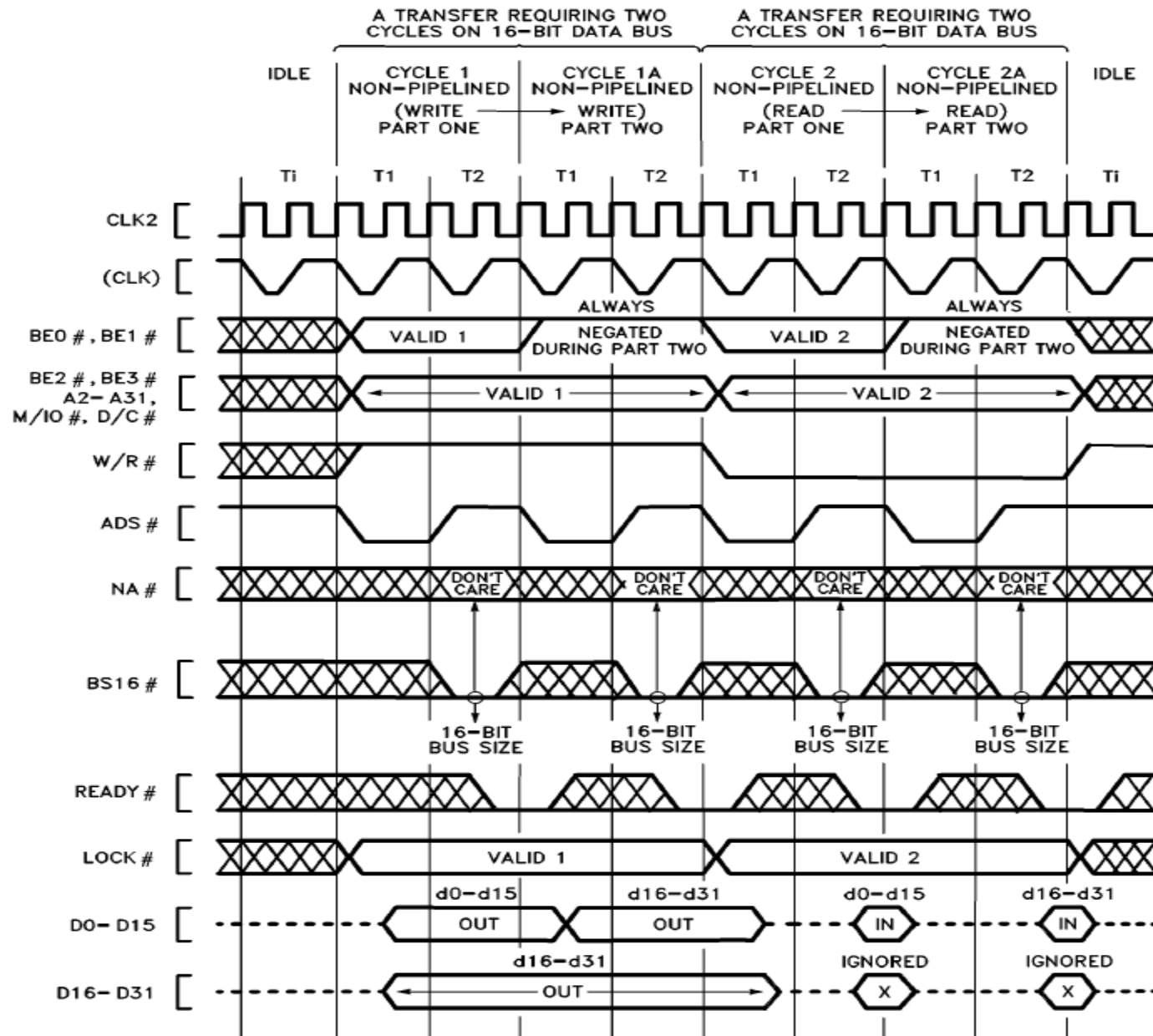


Bus States

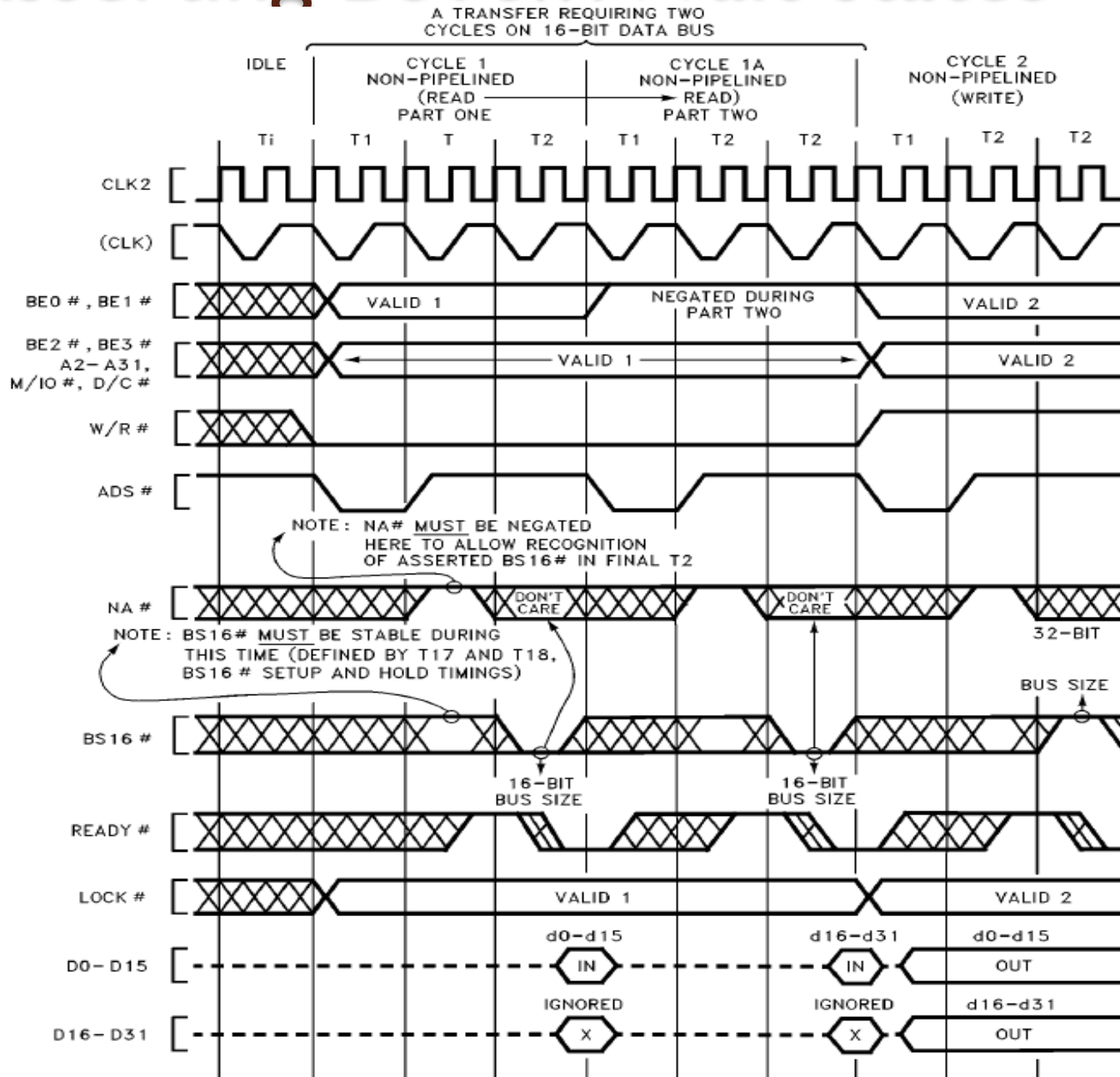
Continued...

- T1: First clock of a non-pipelined bus cycle (Intel386 DX drives new address and asserts ADS#)
- T2: subsequent clocks of a bus cycle when NA# has not been sampled asserted in the current bus cycle
- Ti: idle state
- Th: Hold acknowledge state (Intel386 DX asserts HLDA)
- The fastest bus cycle consists of two states: T1 and T2.

Asserting BS16#: No wait states



Asserting BS16#: Wait states



Pipelined Address

- Address pipelining is the option of requesting the address and the bus cycle definition of the next, internally pending bus cycle before the current bus cycle is acknowledged with **READY#** asserted.
- Following any idle bus state (T_i), addresses are non-pipelined. Within non-pipelined bus cycles, **NA#** is only sampled during wait states.
- Therefore, to begin address pipelining during a group of non-pipelined bus cycles requires a non-pipelined cycle with at least one wait state

Pipelined Address

- Once a bus cycle is in progress and the current address has been valid for at least one entire bus state, the NA# input is sampled at the end of every phase one until the bus cycle is acknowledged
- If NA# is sampled asserted, the Intel386 DX is free to drive the address and bus cycle definition of the next bus cycle, and assert ADS#, as soon as it has a bus request internally pending. It may drive the next address as early as the next bus state, whether the current bus cycle is acknowledged at that time or not.

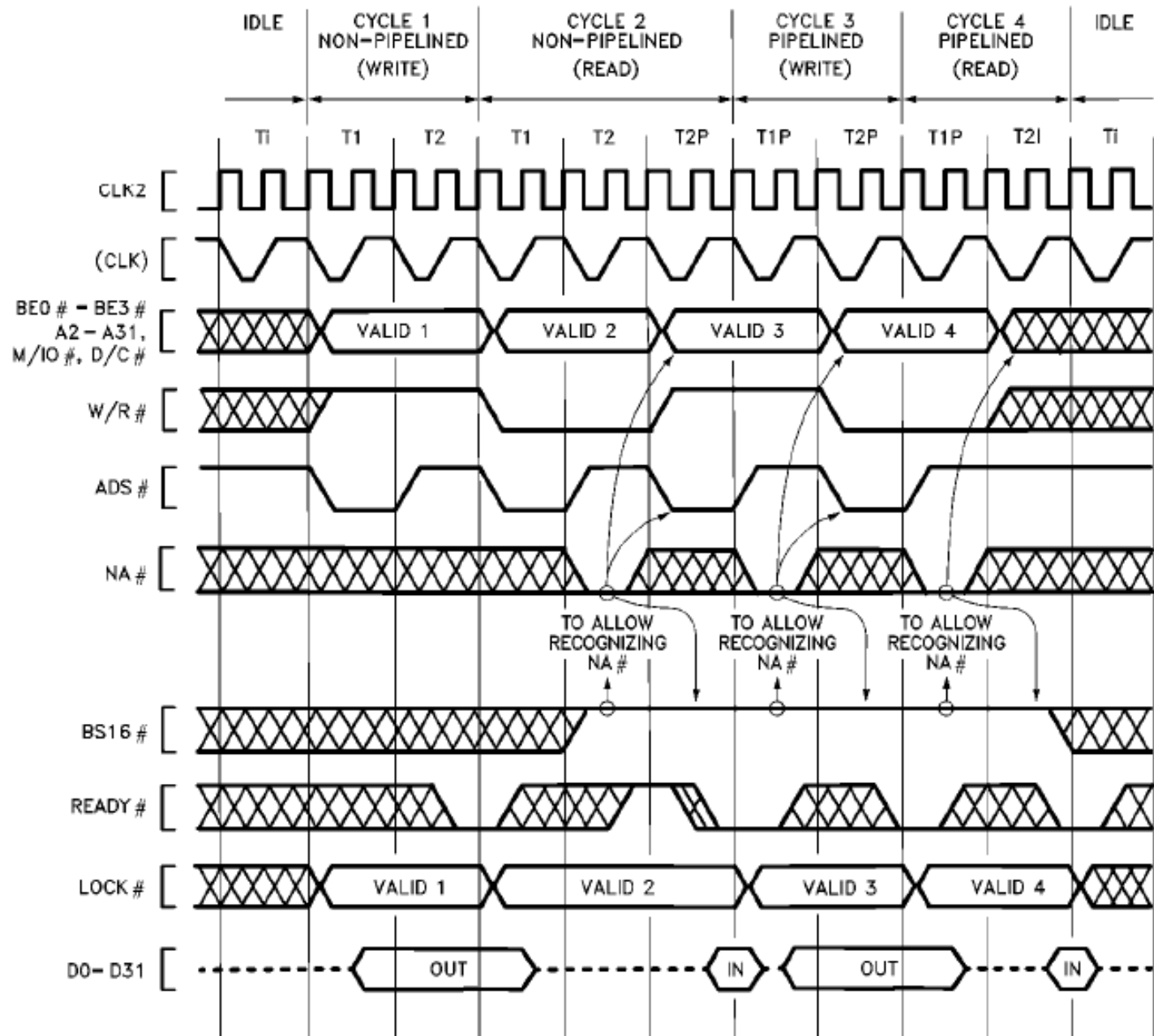
80386DX Characteristics of address pipelining

- For NA# to be sampled asserted, BSI6# must be negated at that sampling window. If NA# and BSI6# are both sampled asserted during the last T2 period of a bus cycle, BSI6# asserted has priority.
- The next address may appear as early as the bus state after NA# was sampled asserted
- Any address which is validated by a pulse on the Intel386 DX ADS# output will remain stable on the address pins for at least two processor clock periods.

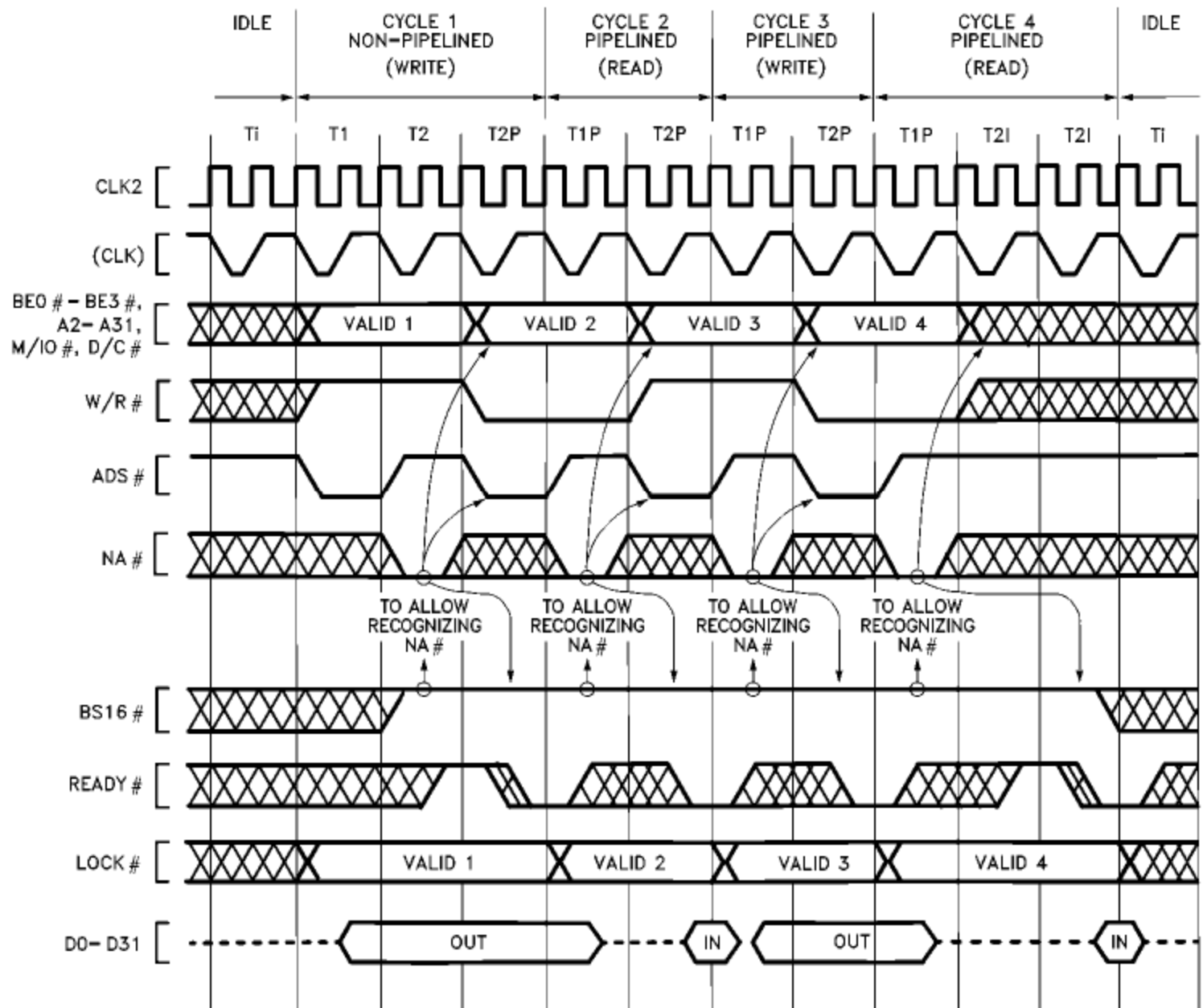
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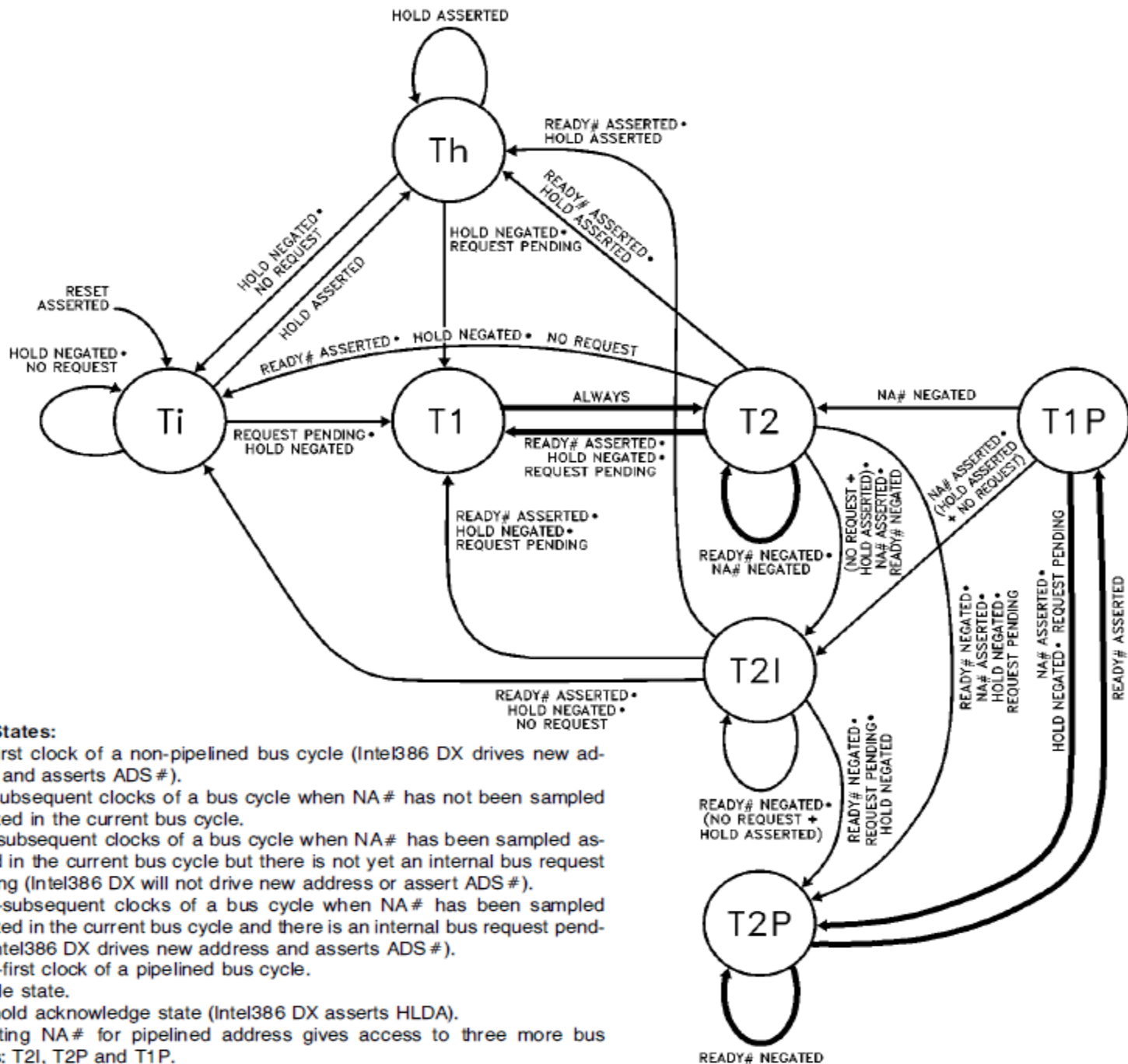
- Once NA# is sampled asserted, the Intel386 DX commits itself to the highest priority bus request that is pending internally. It can no longer perform another 16-bit transfer to the same address should BS16# be asserted externally, so thereafter must assume the current bus size is 32 bits.
- Only the address and bus cycle definition of the very next bus cycle is available.

Transitioning to pipelined address



Fast Transitioning to pipelined address





Bus States

- T1: first clock of a non-pipelined bus cycle (Intel386 DX drives new address and asserts ADS#).
- T2: subsequent clocks of a bus cycle when NA# has not been sampled asserted in the current bus cycle.
- T2I: subsequent clocks of a bus cycle when NA# has been sampled asserted in the current bus cycle but there is not yet an internal bus request pending (Intel386 DX will not drive new address or assert ADS#).
- T2P: subsequent clocks of a bus cycle when NA# has been sampled asserted in the current bus cycle and there is an internal bus request pending (Intel386 DX drives new address and asserts ADS#).
- T1P: first clock of a pipelined bus cycle.
- Ti: idle state.
- Th: hold acknowledge state (Intel386 DX asserts HLDA).
- Asserting NA# for pipelined address gives access to three more bus states: T2I, T2P and T1P.
- Using pipelined address, the fastest bus cycle consists of T1P and T2P

Reference

- Intel ® 80386 Data Sheet. Dec-1993
Order number: 231630

Thank you !